

1 CLAIMS:

2 1. A radio frequency identification device comprising:  
3 a monolithic integrated circuit including a receiver, a transmitter,  
4 and a microprocessor.

5  
6 2. A radio frequency identification device in accordance with  
7 claim 1 wherein the receiver and transmitter together define an active  
8 transponder, and wherein the device comprises a battery supplying power  
9 to the integrated circuit.

10  
11 3. A radio frequency identification device comprising:  
12 a monolithic integrated circuit including a receiver, a transmitter  
13 which can operate at frequencies above 400 MHz, and a microprocessor.

14  
15 4. A radio frequency identification device comprising:  
16 a monolithic integrated circuit including a receiver, a transmitter  
17 which can operate at frequencies above 1 GHz, and a microprocessor.

18  
19 5. A radio frequency identification device comprising:  
20 a monolithic integrated circuit including a transmitter, a  
21 microprocessor, and a receiver which can receive and interpret signals  
22 having frequencies above 400 MHz.  
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1        6.    A radio frequency identification device comprising:  
2        a monolithic integrated circuit including a transmitter, a  
3        microprocessor, and a receiver which can receive and interpret signals  
4        having frequencies above 1 GHz.

5  
6        7.    A radio frequency identification device comprising:  
7        a monolithic integrated circuit including a receiver, a microwave  
8        transmitter, and a microprocessor.

9  
10       8.    A radio frequency identification device in accordance with  
11       claim 7 wherein the receiver and transmitter together define an active  
12       transponder.

13  
14       9.    A radio frequency identification device in accordance with  
15       claim 7 wherein the receiver is a microwave receiver.

16  
17       10.   A radio frequency identification device comprising:  
18       a monolithic integrated circuit including a microwave receiver, a  
19       transmitter, and a microprocessor.

20  
21       11.   A radio frequency identification device in accordance with  
22       claim 10 wherein the receiver and transmitter together define an active  
23       transponder.  
24

1 12. A radio frequency identification device in accordance with  
2 claim 10 wherein the transmitter is a microwave transmitter.

3  
4 13. A radio frequency identification device comprising:  
5 a single die including a receiver, a transmitter, and a  
6 microprocessor, the die having a size less than 90,000 mils<sup>2</sup>.

7  
8 14. A radio frequency identification device in accordance with  
9 claim 13 wherein the die has a size less than 300 x 300 mils<sup>2</sup>.

10  
11 15. A radio frequency identification device in accordance with  
12 claim 13 wherein the die has a size less than 37,500 mils<sup>2</sup>.

13  
14 16. A radio frequency identification device in accordance with  
15 claim 13 wherein the die has a size less than 250 x 150 mils<sup>2</sup>.

16  
17 17. A radio frequency identification device comprising:  
18 a single die including a receiver, a transmitter, and a  
19 microprocessor, the die having a size of substantially 209 by substantially  
20 116 mils<sup>2</sup>.

21  
22 18. A radio frequency identification device comprising:  
23 a single die integrated circuit including a receiver, a transmitter,  
24 and a microprocessor.

1 19. A radio frequency identification device in accordance with  
2 claim 18 wherein the receiver and transmitter together define an active  
3 transponder, and wherein the device comprises a battery supplying power  
4 to the integrated circuit.

5  
6 20. A radio frequency identification device comprising:  
7 a single die with a single metal layer including a receiver, a  
8 transmitter, and a microprocessor.

9  
10 21. A radio frequency identification device in accordance with  
11 claim 20 wherein the receiver and transmitter together define an active  
12 transponder, and wherein the device comprises a battery supplying power  
13 to the integrated circuit.

14  
15 22. A radio frequency identification device comprising:  
16 a single die integrated circuit including a receiver, a transmitter,  
17 and a microprocessor formed using a single metal layer processing  
18 method.

19  
20 23. A radio frequency identification device in accordance with  
21 claim 22 wherein the receiver and transmitter together define an active  
22 transponder, and wherein the device comprises a battery supplying power  
23 to the integrated circuit.

1 24. A radio frequency identification system comprising:  
2 an integrated circuit including a receiver, and a transmitter; and  
3 an antenna coupled to the integrated circuit, the integrated circuit  
4 being responsive to radio frequency signals of multiple carrier  
5 frequencies.

6  
7 25. A radio frequency identification system in accordance with  
8 claim 24 wherein the receiver comprises a Schottky diode detector.

9  
10 26. A radio frequency identification system in accordance with  
11 claim 24 wherein the transmitter comprises a modulated backscatter  
12 transmitter.

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14 27. A radio frequency identification system in accordance with  
15 claim 24 wherein the integrated circuit receives commands from an  
16 interrogator transmitting a radio frequency signal including a series of  
17 digital data bits modulated on a carrier, the carrier having a carrier  
18 frequency, wherein the integrated circuit uses the frequency of data bits  
19 modulated on the carrier but does not use the carrier frequency.  
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1 28. A radio frequency identification device comprising:  
2 transponder circuitry formed in a monolithic integrated circuit  
3 comprising both transmitting and receiving circuits of the transponder  
4 circuitry;  
5 a power supply operably associated with the transponder circuitry;  
6 and  
7 an antenna operably associated with the transponder circuitry.  
8

9 29. A radio frequency identification device comprising:  
10 a monolithic semiconductor integrated circuit including a receiver  
11 and a transmitter;  
12 means for applying a supply of power to the integrated circuit  
13 device from a battery; and  
14 means for configuring the integrated circuit to receive and transmit  
15 radio frequency signals.  
16

17 30. A method for producing a radio frequency identification  
18 device (RFID), the method comprising the following steps:  
19 providing a monolithic integrated circuit having a receiver and a  
20 transmitter; and  
21 providing a package configured to carry the integrated circuit.  
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1        31. A method in accordance with claim 30, the configuring step  
2 including providing an antenna coupled with the integrated circuit and  
3 configurable to enable at least one of signal transmitting and signal  
4 receiving.

5  
6        32. A method for adapting a radio frequency data  
7 communication device for use at a desired carrier frequency for use in  
8 a radio frequency identification (RFID) device, the method comprising  
9 the following steps:

10        providing an integrated circuit having tunable circuitry, the  
11 integrated circuit comprising a receiver and a transmitter;

12        configuring the integrated circuit for connection with a power  
13 supply to enable operation;

14        configuring the integrated circuit to receive and apply radio  
15 frequency signals via an antenna, the antenna and the tunable circuitry  
16 cooperating in operation there between; and

17        tuning the tunable circuitry and the antenna to realize a desired  
18 carrier frequency from a wide range of possible carrier frequencies.  
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1 33. A method for adapting a radio frequency data  
2 communication device for use at a desired carrier frequency for use in  
3 a radio frequency identification (RFID) device, the method comprising  
4 the following steps:

5 providing an integrated circuit having tunable circuitry, the  
6 integrated circuit comprising a receiver and a transmitter;

7 configuring the integrated circuit for connection with a power  
8 supply to enable operation;

9 configuring the integrated circuit to receive and apply radio  
10 frequency signals via an antenna, the antenna and the tunable circuitry  
11 cooperating in operation there between; and

12 tuning the antenna to realize a desired carrier frequency from a  
13 wide range of possible carrier frequencies.

14  
15 34. A radio frequency communications device comprising:

16 an integrated circuit including a transmitter and a receiver, the  
17 integrated circuit including a clock recovery circuit recovering a clock  
18 frequency from a signal received by the receiver, the clock recovery  
19 circuit having a phase lock loop including a voltage controlled oscillator,  
20 and a loop filter having a capacitor storing a voltage indicative of a  
21 frequency at which the voltage controlled oscillator is oscillating, the  
22 integrated circuit using the voltage stored on the capacitor to generate  
23 a clock frequency for the transmitter.  
24



1 35. A radio frequency communications device in accordance with  
2 claim 34 and further comprising circuitry using the voltage stored on the  
3 capacitor to produce a clock signal for generating a transmitter carrier  
4 frequency.

5  
6 36. A radio frequency communications device in accordance with  
7 claim 34 wherein the transmitter transmits using differential phase shift  
8 keying, and further comprising circuitry using the voltage stored on the  
9 capacitor to produce a clock signal, and divider circuitry dividing the  
10 clock frequency to generate tones for differential phase shift keyed  
11 transmission.

1 37. A method of recovering a clock frequency from a received  
2 radio frequency signal, storing the clock frequency, and using the clock  
3 frequency for radio frequency transmission by a transmitter, the method  
4 comprising:

5 providing a clock recovery circuit recovering a clock frequency  
6 from a signal received by the receiver, the clock recovery circuit having  
7 a phase lock loop including a voltage controlled oscillator, and a loop  
8 filter having a capacitor;

9 using the clock recovery circuit to recover a clock frequency from  
10 a received radio frequency signal;

11 storing on the capacitor a voltage indicative of frequency at which  
12 the voltage controlled oscillator is oscillating;

13 using the voltage stored on the capacitor to generate a clock  
14 frequency for use by the transmitter.

15  
16 38. A method in accordance with claim 37 and further  
17 comprising the step using the voltage stored on the capacitor to  
18 produce a clock signal for generating a transmitter carrier frequency.

19  
20 39. A method in accordance with claim 37 and further  
21 comprising the step of using the voltage stored on the capacitor to  
22 produce a clock signal for generating tones for frequency shift keyed  
23 transmission.  
24

1 40. A method in accordance with claim 37 and further  
2 comprising the step of dividing the recovered clock frequency for  
3 generating tones for differential phase shift keyed transmission.  
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6 41. A method of recovering and storing a clock frequency from  
7 a received radio frequency signal in a radio frequency identification  
8 device including a transmitter and a receiver, the method comprising:

9 providing a clock recovery circuit recovering a clock frequency  
10 from a signal received by the receiver, the clock recovery circuit having  
11 a phase lock loop;

12 using the clock recovery circuit to recover a clock frequency from  
13 a received radio frequency signal;

14 storing in analog form a value indicative of frequency at which  
15 the voltage controlled oscillator is oscillating;

16 using the analog value to generate a clock frequency for use by  
17 the transmitter.  
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1 42. A radio frequency communications device comprising:  
2 an integrated circuit including a transmitter and a receiver, the  
3 transmitter being switchable between a backscatter mode, wherein a  
4 carrier for the transmitter is derived from a carrier received from an  
5 interrogator spaced apart from the radio frequency communications  
6 device, and an active mode, wherein a carrier for the transmitter is  
7 generated by the integrated circuit itself.  
8

9 43. A radio frequency communications device in accordance with  
10 claim 42 wherein the transmitter switches between the backscatter and  
11 active modes in response to a radio frequency command received by the  
12 receiver.  
13

14 44. A radio frequency communications device comprising:  
15 an integrated circuit including a transmitter and a receiver, the  
16 transmitter selectively transmitting a signal using a modulation scheme,  
17 the transmitter being switchable for transmission using different  
18 modulation schemes.  
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1 45. A radio frequency communications device in accordance with  
2 claim 44 wherein the transmitter is switchable between at least two  
3 modulation schemes selected from the group consisting of Frequency  
4 Shift Keying (FSK), Binary Phase Shift Keying (BPSK), Direct Sequence  
5 Spread Spectrum, On-Off Keying (OOK), Amplitude Modulation (AM),  
6 and Modulated Backscatter (MBS).

7  
8 46. A method for adapting modulation schemes of a radio  
9 frequency data communication device in a radio frequency identification  
10 (RFID) device, the method comprising the following steps:

11 providing an integrated circuit having switching circuitry, a receiver,  
12 a transmitter, and a processor; the integrated circuit having a plurality  
13 of transmitting circuits including a first transmitting circuit configured  
14 to realize an active transmitter scheme and a second transmitting circuit  
15 configured to realize a modulated backscatter scheme;

16 configuring the integrated circuit for connection with a power  
17 supply to enable operation;

18 configuring the integrated circuit to receive and apply radio  
19 frequency signals via an antenna, the antenna and the tunable circuitry  
20 cooperating in operation; and

21 switching the switchable circuitry with respect to the antenna to  
22 enable one of the transmitting circuits to realize one of the modulation  
23 schemes.  
24

1 47. A method for adapting modulation schemes of a radio  
2 frequency data communication device in a radio frequency identification  
3 (RFID) device, the method comprising the following steps:

4 providing an integrated circuit having switching circuitry, a receiver,  
5 a transmitter, and a processor, the integrated circuit including a plurality  
6 of transmitting circuits, the plurality of transmitting circuits configured  
7 to selectively realize a plurality of modulated backscatter schemes;

8 configuring the integrated circuit for connection with a power  
9 supply to enable operation;

10 configuring the integrated circuit to receive and apply radio  
11 frequency signals via an antenna, the antenna and the tunable circuitry  
12 cooperating in operation; and

13 switching the transmitting circuits with respect to the antenna to  
14 enable one of the transmitting circuits to realize one of the modulation  
15 schemes.

16  
17 48. A radio frequency identification device comprising:

18 an integrated circuit including a transmitter and a receiver, the  
19 integrated circuit being adapted to be connected to a battery, and  
20 further including a comparator comparing the voltage of the battery with  
21 a predetermined voltage and generating a low battery signal if the  
22 voltage of the battery is less than the predetermined voltage.

1 49. A radio frequency identification device in accordance with  
2 claim 48 wherein the integrated circuit further comprises a band gap  
3 voltage generator which generates a reference voltage, and wherein the  
4 predetermined voltage is the reference voltage produced by the band  
5 gap voltage generator.  
6

7 50. A radio frequency identification device in accordance with  
8 claim 48 wherein the integrated circuit responds to commands received  
9 by the receiver from an interrogator, wherein the integrated circuit  
10 comprises a status register having a value indicating whether battery  
11 voltage is less than the predetermined voltage and wherein the  
12 transmitter transmits the value of the status register in response to a  
13 command received by the receiver.  
14

15 51. A radio frequency identification device in accordance with  
16 claim 48 wherein the transmitter selectively transmits the low battery  
17 signal using a radio frequency signal.  
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1        52. A method for detecting a low battery condition in a radio  
2 frequency data communication device for use in a radio frequency  
3 identification (RFID) device, the method comprising the following steps:

4        providing an integrated circuit having switching circuitry, a receiver,  
5 and a transmitter, the integrated circuit including a comparator  
6 configured to compare the battery voltage with a predetermined voltage  
7 and generate a low battery signal if the battery voltage is less than the  
8 predetermined voltage;

9        configuring the integrated circuit for connection with the battery  
10 to enable operation;

11        configuring the integrated circuit to receive and apply radio  
12 frequency signals via an antenna, the antenna and the tunable circuitry  
13 cooperating in operation there between;

14        determining a predetermined voltage for the battery;

15        comparing the voltage of the battery with the predetermined  
16 voltage; and

17        generating a low battery signal if the voltage of the battery is  
18 less than the predetermined voltage.  
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1        53. A radio frequency communications device comprising:  
2        an integrated circuit including a transmitter and a receiver, the  
3        integrated circuit periodically checking if a radio frequency signal is  
4        being received by the receiver, the integrated circuit further including  
5        a timer setting a time period for the checking, the timer having a  
6        frequency lock loop.

7  
8        54. A radio frequency communications device in accordance with  
9        claim 53 wherein the frequency lock loop comprises a current controlled  
10       oscillator.

11  
12       55. A radio frequency communications device in accordance with  
13       claim 53 wherein the integrated circuit is configured to recover a clock  
14       frequency from the received signal and wherein the transmitter is  
15       configured to use the recovered clock frequency.

16  
17       56. A radio frequency communications device in accordance with  
18       claim 53 wherein the integrated circuit switches between a sleep mode,  
19       and a higher power mode in which more power is consumed than in  
20       the sleep mode.

1 57. A radio frequency communications device in accordance with  
2 claim 53 and further comprising a variable value divider connected to  
3 the output of the frequency lock loop, the value of the divider being  
4 programmable in response to a radio frequency signal received by the  
5 receiver so as to program the time period of the checking.  
6

7 58. A radio frequency communications device in accordance with  
8 claim 53 wherein the device is configured to receive and process  
9 commands from an interrogator transmitting a radio frequency signal and  
10 to enable the frequency lock loop only during processing of a command,  
11 to calibrate the timer to a clock frequency recovered from a received  
12 command.  
13

14 59. A radio frequency communications device comprising:  
15 an integrated circuit including a transmitter and a receiver, the  
16 integrated circuit being configured to periodically check if a radio  
17 frequency signal is being received by the receiver, the integrated circuit  
18 further including a timer setting a time period for the checking, the  
19 timer having a phase lock loop.  
20

21 60. A radio frequency communications device in accordance with  
22 claim 59 wherein a clock frequency is recovered from the received  
23 signal and used by the transmitter.  
24

1           61. A radio frequency communications device in accordance with  
2 claim 59 wherein the phase lock loop comprises a current controlled  
3 oscillator.

4  
5           62. A radio frequency communications device in accordance with  
6 claim 59 wherein the integrated circuit switches between a sleep mode,  
7 and a higher power mode in which more power is consumed than in  
8 the sleep mode.

9  
10          63. A radio frequency communications device in accordance with  
11 claim 59 and further comprising a variable value divider connected to  
12 the output of the phase lock loop, the value of the divider being  
13 programmable in response to a radio frequency signal received by the  
14 receiver so as to program the time period for the checking.

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16          64. A radio frequency communications device in accordance with  
17 claim 59 wherein the device receives and processes commands from an  
18 interrogator transmitting a radio frequency signal, and wherein the phase  
19 lock loop is enabled only during processing of a command, to calibrate  
20 the timer to a clock frequency recovered from a received command.

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1        65. A method for calibrating a clock in a radio frequency data  
2 communication device for use in a radio frequency identification (RFID)  
3 device, the method comprising the following steps:

4        providing an integrated circuit having a receiver and a transmitter,  
5 the integrated circuit including a timer having a frequency lock loop  
6 configured to set a time period for periodically checking if a radio  
7 frequency signal is being received by the receiver;

8        configuring the integrated circuit for connection with a battery to  
9 enable operation;

10       configuring the integrated circuit to receive and apply radio  
11 frequency signals via an antenna, the antenna and the integrated circuit  
12 cooperating in operation therebetween; and

13       periodically checking whether a radio frequency signal is being  
14 received by the receiver.

15  
16       66. A radio frequency identification device for receiving and  
17 responding to radio frequency commands from an interrogator  
18 transmitting a radio frequency signal, the device comprising:

19       an integrated circuit including a receiver, a transmitter, and a  
20 connection pin, the integrated circuit being switchable between a radio  
21 frequency receive mode wherein the receiver receives commands via  
22 radio frequency, and a direct receive mode wherein commands are  
23 received via the connection pin.

1 67. A radio frequency identification device in accordance with  
2 claim 66 wherein the connection pin is a serial input pin.  
3

4 68. A radio frequency identification device in accordance with  
5 claim 66 and further comprising a selection pin, and wherein the  
6 integrated circuit switches between the radio frequency receive mode and  
7 the direct receive mode in response to a signal applied to the selection  
8 pin.  
9

10 69. A radio frequency identification device for receiving and  
11 responding to radio frequency commands from an interrogator  
12 transmitting a radio frequency signal, the device comprising:

13 an integrated circuit including a receiver, a transmitter, and a  
14 digital input pin, the integrated circuit being switchable between a radio  
15 frequency receive mode wherein the receiver receives commands via  
16 radio frequency, and a direct receive mode wherein commands are  
17 received digitally via the digital input pin.  
18

19 70. A radio frequency identification device in accordance with  
20 claim 69 wherein the digital input pin is a serial input pin.  
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1        71. A radio frequency identification device in accordance with  
2 claim 69 and further comprising a selection pin, and wherein the  
3 integrated circuit switches between the radio frequency receive mode and  
4 the direct receive mode in response to a signal applied to the selection  
5 pin.

6  
7        72. A radio frequency identification device for receiving  
8 and responding to radio frequency commands from an interrogator  
9 transmitting a radio frequency signal, the device comprising:

10        an integrated circuit including a receiver, a transmitter, and a  
11 connection pin, the integrated circuit being switchable between a radio  
12 frequency receive mode wherein the receiver receives commands via  
13 radio frequency, and a direct receive mode wherein a modulation signal  
14 without a carrier is received via the connection pin.

15  
16        73. A radio frequency identification device in accordance with  
17 claim 72 wherein the connection pin is a serial input pin.

18  
19        74. A radio frequency identification device in accordance with  
20 claim 72 and further comprising a selection pin, and wherein the  
21 integrated circuit switches between the radio frequency receive mode and  
22 the direct receive mode in response to a signal applied to the selection  
23 pin.

1        75. A radio frequency identification device for receiving and  
2        responding to radio frequency commands from an interrogator  
3        transmitting a radio frequency signal, the device comprising:

4        an integrated circuit including a receiver, a transmitter, and a  
5        connection pin, the integrated circuit being switchable between a radio  
6        frequency transmit mode wherein the receiver transmits responses to the  
7        commands via radio frequency, and a direct transmit mode wherein  
8        responses are transmitted via the connection pin.

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10       76. A radio frequency identification device in accordance with  
11       claim 75 wherein the connection pin is a serial output pin.

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13       77. A radio frequency identification device in accordance with  
14       claim 75 and further comprising a selection pin, and wherein the  
15       integrated circuit switches between the radio frequency transmit mode  
16       and the direct transmit mode in response to a signal applied to the  
17       selection pin.

1 78. A radio frequency identification device for receiving and  
2 responding to radio frequency commands from an interrogator  
3 transmitting a radio frequency signal, the device comprising:

4 an integrated circuit including a receiver, a transmitter, and a  
5 digital output pin, the integrated circuit being switchable between a  
6 radio frequency transmit mode wherein the receiver transmits responses  
7 to the commands via radio frequency, and a direct transmit mode  
8 wherein responses are transmitted digitally via the digital output pin.  
9

10 79. A radio frequency identification device in accordance with  
11 claim 78 wherein the connection pin is a serial output pin.  
12

13 80. A radio frequency identification device in accordance with  
14 claim 78 and further comprising a selection pin, and wherein the  
15 integrated circuit switches between the radio frequency transmit mode  
16 and the direct transmit mode in response to a signal applied to the  
17 selection pin.  
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1        81. A radio frequency identification device for receiving and  
2        responding to radio frequency commands from an interrogator  
3        transmitting a radio frequency signal, the device comprising:

4        an integrated circuit including a receiver, a transmitter, and a  
5        connection pin, the integrated circuit being switchable between a radio  
6        frequency transmit mode wherein the receiver transmits responses to the  
7        commands via radio frequency, and a direct transmit mode wherein a  
8        modulation signal without a carrier is transmitted via the connection pin.

9  
10       82. A radio frequency identification device in accordance with  
11       claim 81 wherein the connection pin is a serial output pin.

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13       83. A radio frequency identification device in accordance with  
14       claim 81 and further comprising a selection pin, and wherein the  
15       integrated circuit switches between the radio frequency transmit mode  
16       and the direct transmit mode in response to a signal applied to the  
17       selection pin.

1 84. A method comprising the following steps:

2 providing an integrated circuit having a receiver, a transmitter, and  
3 a connection pin, the integrated circuit including a switchable circuit  
4 configured to switch between a radio frequency receive mode wherein  
5 the receiver receives commands via radio frequency, and a direct receive  
6 mode wherein commands are received via the connection pin;

7 configuring the integrated circuit for connection with a battery;

8 configuring the integrated circuit to receive and transmit radio  
9 frequency signals via an antenna, the antenna and the integrated circuit  
10 cooperating in operation; and

11 switching to one of the radio frequency receive mode and the  
12 direct receive mode to enable receipt of radio frequency commands or  
13 commands received via the connection pin.

1 85. A method comprising the following steps:

2 providing an integrated circuit having a receiver, a transmitter, and  
3 a connection pin, the integrated circuit including a switchable circuit  
4 configured to switch between a radio frequency transmit mode wherein  
5 the transmitter transmits information via radio frequency, and a direct  
6 transmit mode wherein data is transmitted via the connection pin;

7 configuring the integrated circuit for connection with a battery;

8 configuring the integrated circuit to receive and transmit radio  
9 frequency signals via an antenna, the antenna and the integrated circuit  
10 cooperating in operation; and

11 switching to one of the radio frequency transmit mode and the  
12 direct transmit mode to enable transmission of information via radio  
13 frequency or via the connection pin.

14  
15 86. An integrated circuit comprising:

16 a radio frequency receiver;

17 a unique, non-alterable indicia identifying the integrated circuit;

18 and

19 a radio frequency transmitter configured to transmit a signal  
20 representative of the indicia in response to a command received by the  
21 receiver.  
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1        87. An integrated circuit in accordance with claim 86 and  
2 further comprising an antenna coupled to the integrated circuit, a  
3 battery coupled to the integrated circuit and powering the integrated  
4 circuit, and a tag housing encapsulating the integrated circuit, battery,  
5 and antenna.

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7        88. An integrated circuit in accordance with claim 86 wherein  
8 the integrated circuit comprises a programmable read only memory, and  
9 wherein the non-alterable indicia is burned into the programmable read  
10 only memory.

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12        89. An integrated circuit in accordance with claim 86 wherein  
13 the non-alterable indicia comprises laser blown polysilicon links.

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15        90. An integrated circuit in accordance with claim 86 wherein  
16 the integrated circuit comprises an EEPROM containing the non-alterable  
17 indicia.

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19        91. An integrated circuit in accordance with claim 86 wherein  
20 the integrated circuit comprises a flash ROM containing the non-  
21 alterable indicia.

1 92. A radio frequency identification device comprising:  
2 an integrated circuit including a receiver for receiving radio  
3 frequency commands from an interrogation device, and a transmitter for  
4 transmitting a signal identifying the device to the interrogator, the  
5 transmitter and receiver being formed on a die having a lot number,  
6 wafer number, and die number, the integrated circuit including non-  
7 alterable indicia identifying the lot number, wafer number, and die  
8 number, the transmitter being configured to transmit the non-alterable  
9 indicia in response to a manufacturer's command received by the  
10 receiver, the transmitted non-alterable indicia being different from the  
11 identifying signal.

12  
13 93. A radio frequency identification device in accordance with  
14 claim 92 wherein the integrated circuit comprises a programmable read  
15 only memory, and wherein the non-alterable indicia is burned into the  
16 programmable read only memory.

17  
18 94. An integrated circuit in accordance with claim 92 wherein  
19 the non-alterable indicia comprises laser blown polysilicon links.  
20

21 95. An integrated circuit in accordance with claim 92 wherein  
22 the integrated circuit comprises an EEPROM containing the non-alterable  
23 indicia.  
24

1           96. An integrated circuit in accordance with claim 92 wherein  
2 the integrated circuit comprises a flash ROM containing the non-  
3 alterable indicia.

4  
5           97. A radio frequency identification device in accordance with  
6 claim 92 and further comprising an antenna coupled to the integrated  
7 circuit, a battery coupled to the integrated circuit and powering the  
8 integrated circuit, and a tag housing encapsulating the integrated circuit,  
9 battery, and antenna.

10  
11           98. A method of tracing manufacturing process problems by  
12 tracing the origin of a defective radio frequency identification integrated  
13 circuit, the method comprising:

14           forming a non-alterable indicia on a die for the integrated circuit,  
15 the indicia representing the wafer lot number, wafer number, and die  
16 number on the wafer, the indicia being not readily ascertainable by a  
17 user; and

18           causing the integrated circuit to transmit the non-alterable indicia  
19 via radio frequency in response to a manufacturer's command.  
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1 99. A method of tracing stolen property including a radio  
2 frequency identification integrated circuit, the method comprising:

3 forming a non-alterable indicia on a die for the integrated circuit,  
4 the indicia representing the wafer lot number, wafer number, and die  
5 number on the wafer, the indicia being not readily ascertainable by a  
6 user; and

7 causing the integrated circuit to transmit the non-alterable indicia  
8 via radio frequency in response to a manufacturer's command.

9  
10 100. A method of tracing manufacturing process problems in the  
11 manufacture of a radio frequency integrated circuit by tracing defect  
12 origin, the method comprising the following steps:

13 providing a detectable signature on the integrated circuit, the  
14 signature indicative of one or more of the wafer lot number, wafer  
15 number, and die number of a die for the integrated circuit; and

16 enabling the integrated circuit to transmit the signature via radio  
17 frequency responsive to an inquiry command.

1        101. A radio frequency identification device comprising:  
2        an integrated circuit including a microprocessor, a receiver  
3        receiving radio frequency commands from an interrogation device, and  
4        a transmitter transmitting a signal identifying the device to the  
5        interrogator, the integrated circuit switching between a sleep mode, and  
6        a microprocessor on mode, in which more power is consumed than in  
7        the sleep mode, if the microprocessor determines that a signal received  
8        by the receiver is a radio frequency command from an interrogation  
9        device.  
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1           102. A method for conserving power during operation of a radio  
2 frequency identification device (RFID), the method comprising the  
3 following steps:

4           providing a receiver, a transmitter, microprocessor, and wake-up  
5 circuitry, the wake-up circuitry configured to selectively supply clock  
6 signals to the processor and thus control power consumption of the  
7 processor;

8           configuring the receiver with an antenna to receive radio frequency  
9 signals from an interrogation device,

10          configuring the transmitter to transmit a signal identifying the  
11 device to the interrogator;

12          selectively enabling powered wake-up of the receiver to periodically  
13 check for presence of radio frequency signals;

14          detecting whether a radio frequency signal is valid; and

15          depending on whether a radio frequency signal is valid, supplying  
16 clock signals to the processor.

17  
18          103. A method in accordance with claim 102 wherein the  
19 receiver, the transmitter, and the wake-up circuitry are provided on an  
20 integrated circuit.  
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1        104. A method for conserving power during operation of a radio  
2 frequency identification device (RFID), the method comprising the  
3 following steps:

4        providing a receiver, a transmitter, microprocessor, and wake-up  
5 circuitry, the wake-up circuitry configured to selectively supply power to  
6 the processor;

7        configuring the receiver with an antenna to receive radio frequency  
8 signals from an interrogation device,

9        configuring the transmitter to transmit a signal identifying the  
10 device to the interrogator;

11        selectively enabling powered wake-up of the receiver to periodically  
12 check for presence of radio frequency signals;

13        detecting whether a radio frequency signal is valid; and

14        depending on whether a radio frequency signal is valid, supplying  
15 power signals to the processor.

16  
17        105. A method in accordance with claim 104 wherein the  
18 receiver, the transmitter, and the wake-up circuitry are provided on an  
19 integrated circuit.  
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1 106. A radio frequency identification device comprising:  
2 an integrated circuit including a microprocessor, a transmitter, and  
3 a receiver, the integrated circuit being switchable between a sleep mode,  
4 and a microprocessor on mode in which more power is consumed than  
5 in the sleep mode, the integrated circuit being switched from the sleep  
6 mode to the microprocessor on mode in response to a direct sequence  
7 spread spectrum modulated radio frequency signal, which has a  
8 predetermined number of transitions within a certain period of time,  
9 being received by the receiver.  
10

11 107. A method for conserving power in a radio frequency  
12 identification device, the method comprising periodically switching from  
13 a sleep mode to a receiver on mode and performing the following tests  
14 to determine whether to further switch to a microprocessor on mode  
15 because a valid radio frequency signal is present:

16 (a) determining if any radio frequency signal is present and, if  
17 so, proceeding to step (b); and, if not, returning to the sleep mode;  
18 and

19 (b) determining if the radio frequency signal has a  
20 predetermined number of transitions per a predetermined time period  
21 and, if so, switching to the microprocessor on mode; and, if not,  
22 returning to the sleep mode.  
23  
24

1        108. A method in accordance with claim 107 wherein the radio  
2 frequency identification device further comprises a clock recovery circuit  
3 recovering a clock from incoming radio frequency signals, the clock  
4 recovery circuit including a phase lock loop and wherein the tests  
5 further comprise determining whether frequency lock is achieved on the  
6 incoming radio frequency signal within a predetermined number of  
7 transitions.

8  
9        109. A radio frequency identification device switchable between  
10 a sleep mode and a mode in which more power is consumed than in  
11 the sleep mode, the radio frequency identification device comprising:

12        a transponder including a receiver and a transmitter;

13        means for periodically checking whether any radio frequency signal  
14 is being received by the receiver; and

15        means for determining if a radio frequency signal has a  
16 predetermined number of transitions within a predetermined period of  
17 time.

1 110. A method for conserving power in a radio frequency  
2 identification device, the method comprising periodically switching from  
3 a sleep mode to a receiver on mode and performing the following tests  
4 to determine whether to further switch to a microprocessor on mode  
5 because a valid radio frequency signal is present:

6 (a) determining if any radio frequency signal is present and, if  
7 so, proceeding to step (b); and, if not, returning to the sleep mode;

8 (b) determining if the radio frequency signal is modulated and  
9 has a predetermined number of transitions per a predetermined period  
10 of time and, if so, proceeding to step (c); and, if not, returning to the  
11 sleep mode; and

12 (c) determining if the modulated radio frequency signal has a  
13 predetermined number of transitions per a predetermined period of time  
14 different from the predetermined time of step (b) and, if so, switching  
15 to the microprocessor on mode; and, if not, returning to the sleep  
16 mode.

17  
18 111. A method in accordance with claim 110 wherein the radio  
19 frequency identification device further comprises a clock recovery circuit  
20 recovering a clock from incoming radio frequency signals, the clock  
21 recovery circuit including a phase lock loop and wherein the tests  
22 further comprise determining whether frequency lock is achieved on the  
23 incoming radio frequency signal within a predetermined amount of time.  
24

1 112. A method of forming an integrated circuit including a  
2 Schottky diode, the method comprising:

3 providing a p-type substrate;  
4 defining an n-type region relative to the substrate;  
5 forming an insulator over the n-type region;  
6 removing an area of the insulator for definition of a contact hole,  
7 and removing an area encircling the contact hole;  
8 forming n+regions in the n-type regions encircling the contact  
9 hole;  
10 depositing a Schottky metal in the contact hole; and  
11 annealing the metal to form a silicide interface to the n-type  
12 region.

13  
14 113. A method in accordance with claim 112 and further  
15 comprising depositing tungsten into the contact hole.

16  
17 114. A method in accordance with claim 113 wherein the  
18 tungsten is deposited by chemical vapor deposition.

19  
20 115. A method in accordance with claim 113 and further  
21 comprising planarizing the tungsten.  
22  
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24

1 116. A method of forming an integrated circuit including a  
2 Schottky diode, the method comprising:

3 providing a substrate;  
4 defining a p-type region relative to the substrate;  
5 forming an insulator over the p-type region;  
6 removing an area of the insulator for definition of a contact hole,  
7 and removing an area encircling the contact hole;  
8 forming p<sup>+</sup>regions in the p-type regions encircling the contact  
9 hole;  
10 depositing a Schottky metal in the contact hole; and  
11 annealing the Schottky metal to form a silicide interface to the  
12 p-type region.

13  
14 117. A method in accordance with claim 116 and further  
15 comprising depositing tungsten into the contact hole.

16  
17 118. A method in accordance with claim 117 wherein the  
18 tungsten is deposited by chemical vapor deposition.

19  
20 119. A method in accordance with claim 117 and further  
21 comprising planarizing the tungsten  
22  
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1 120. A method of forming an integrated circuit including a  
2 Schottky diode, the method comprising:

3 providing a p-type substrate;

4 defining an n-well region relative to the substrate;

5 forming a BPSG insulator over the n-well region;

6 etching away an area of the BPSG for definition of a contact  
7 hole, and etching an area encircling the contact hole;

8 forming n+regions in the n-well regions encircling the contact  
9 hole;

10 depositing titanium in the contact hole; and

11 annealing the titanium to form a silicide interface to the n-well  
12 region.

13  
14 121. A method in accordance with claim 120 and further  
15 comprising depositing tungsten into the contact hole.

16  
17 122. A method in accordance with claim 121 wherein the  
18 tungsten is deposited by chemical vapor deposition.

19  
20 123. A method in accordance with claim 121 and further  
21 comprising planarizing the tungsten.



1 124. A method of forming an integrated circuit including a  
2 Schottky diode, the method comprising:

3 providing an n-type substrate;  
4 defining a p-well region relative to the substrate;  
5 forming a BPSG insulator over the p-well region;  
6 etching away an area of the BPSG for definition of a contact  
7 hole, and etching an area encircling the contact hole;  
8 forming p+regions in the p-well regions encircling the contact  
9 hole;  
10 depositing titanium in the contact hole; and  
11 annealing the titanium to form a silicide interface to the p-well  
12 region.

13  
14 125. A method in accordance with claim 124 and further  
15 comprising depositing tungsten into the contact hole.

16  
17 126. A method in accordance with claim 125 wherein the  
18 tungsten is deposited by chemical vapor deposition.

19  
20 127. A method in accordance with claim 125 and further  
21 comprising planarizing the tungsten.

22

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1 128. A radio frequency communications system comprising:  
2 an antenna;  
3 an integrated circuit including a receiver having a Schottky diode  
4 detector including a Schottky diode coupled to the antenna; and  
5 a current source connected to drive current through the antenna  
6 and the Schottky diode.

7  
8 129. A radio frequency communications system in accordance with  
9 claim 128 wherein the receiver is inductorless.

10  
11 130. An integrated circuit for radio frequency communications  
12 comprising an inductorless radio frequency detector.

13  
14 131. A system comprising:  
15 an antenna;  
16 a transponder including a receiver having a Schottky diode  
17 detector including a Schottky diode having a first terminal coupled to  
18 the antenna and having a second terminal; and  
19 means for driving current through both the antenna and the  
20 Schottky diode in a direction from the first terminal to the second  
21 terminal.

1 132. A system comprising:  
2 an antenna;  
3 a transponder including a receiver having a Schottky diode  
4 detector including a Schottky diode having a first terminal coupled to  
5 the antenna and having a second terminal; and  
6 means for driving current through both the antenna and the  
7 Schottky diode in a direction from the second terminal to the first  
8 terminal.

9  
10 133. A system comprising:  
11 an antenna;  
12 a transponder including a receiver having a Schottky diode  
13 detector including a Schottky diode having an anode coupled to the  
14 antenna and having a cathode; and  
15 means for driving current through both the antenna and the  
16 Schottky diode in a direction from the anode to the cathode.

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1 134. A radio frequency communications system comprising:  
2 an antenna;  
3 an integrated circuit including a receiver having a Schottky diode  
4 detector including a Schottky diode having an anode coupled to the  
5 antenna and having a cathode, the Schottky diode detector further  
6 including a capacitor connected between the cathode and ground, and  
7 including a capacitor having a first contact connected to the cathode  
8 and having a second contact defining an output of the Schottky diode  
9 detector;  
10 a current source connected to the cathode to drive current  
11 through the antenna and the Schottky diode in a direction from the  
12 anode to the cathode.

1 135. A radio frequency communications system comprising:  
2 an antenna;  
3 an integrated circuit including a receiver having a Schottky diode  
4 detector including a Schottky diode having a cathode coupled to the  
5 antenna and having an anode, the Schottky diode detector further  
6 including a capacitor connected between the anode and ground, and  
7 including a capacitor having a first contact connected to the anode and  
8 having a second contact defining an output of the Schottky diode  
9 detector; and  
10 a current source connected to the anode to drive current through  
11 the antenna and the Schottky diode in a direction from the anode to  
12 the cathode.

13  
14 136. A system comprising:  
15 an antenna;  
16 a transponder including a receiver having a Schottky diode  
17 detector including a Schottky diode having a cathode coupled to the  
18 antenna and having an anode; and  
19 means for driving current through both the antenna and the  
20 Schottky diode in a direction from the anode to the cathode.  
21  
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1 137. A method for realizing an improved radio frequency detector  
2 for use in a radio frequency identification device (RFID), the method  
3 comprising the following steps:

4 providing an integrated circuit and an antenna, the integrated  
5 circuit having a receiver and a transmitter, the integrated circuit further  
6 having a Schottky diode and a current source, with the Schottky diode  
7 in operation being coupled to the antenna and the current source, the  
8 Schottky diode and antenna cooperating there between to form an  
9 inductorless radio frequency detector;

10 applying a supply of power to the integrated circuit device from  
11 a battery; and

12 applying a desired current across the Schottky diode to impart a  
13 desired impedance there across relative to the impedance of the  
14 antenna.

15  
16 138. A frequency lock loop comprising:

17 a current controlled oscillator including a plurality of selectively  
18 engageable current mirrors, the frequency of oscillation of the frequency  
19 lock loop varying in response to selection of the current mirrors, the  
20 current mirrors including transistors operating in a subthreshold mode.  
21  
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1 139. A frequency lock loop in accordance with claim 138 and  
2 further comprising a current source including a thermal voltage  
3 generator, and wherein the selected current mirrors multiply up the  
4 current from the current source to a current for controlling the  
5 frequency of oscillation.

6  
7 140. A frequency lock loop in accordance with claim 138 wherein  
8 the current mirrors are arranged in selectable groups of varying numbers  
9 of transistors to define a binary weighting scheme.

10  
11 141. A frequency lock loop in accordance with claim 140 and  
12 further comprising digital select lines, and wherein the groups are  
13 selected by signals on the digital select lines.

14  
15 142. An integrated circuit comprising a receiver, a transmitter,  
16 and a frequency lock loop including a current source having a thermal  
17 voltage generator, a current controlled oscillator having a plurality of  
18 selectively engageable current mirrors multiplying up the current of the  
19 current source, the frequency of oscillation of the frequency lock loop  
20 varying in response to selection of the current mirrors, the current  
21 mirrors including transistors operating in a subthreshold mode.

1 143. A frequency lock loop in accordance with claim 142 wherein  
2 the current mirrors are arranged in selectable groups of varying numbers  
3 of transistors to define a binary weighting scheme.

4  
5 144. A frequency lock loop in accordance with claim 143 and  
6 further comprising digital select lines, and wherein the groups are  
7 selected by signals on the digital select lines.

8  
9 145. A timing oscillator that consumes less than one milliAmp.

10  
11 146. A method of constructing a frequency lock loop including  
12 a current controlled oscillator having a plurality of selectively engageable  
13 current mirrors, the frequency of oscillation of the frequency lock loop  
14 varying in response to selection of the current mirrors, the method  
15 comprising selecting current mirrors to vary frequency of operation, and  
16 operating transistors in the current mirrors in subthreshold mode.

17  
18 147. A method in accordance with claim 146 and further  
19 comprising using a current source including a thermal voltage generator,  
20 and arranging the current mirrors so the engaged current mirrors  
21 multiply up the current from the current source to a current for  
22 controlling the frequency of oscillation.



1 148. A method in accordance with claim 146 and further  
2 comprising arranging the current mirrors in selectable groups of varying  
3 numbers of transistors to define a binary weighting scheme.

4  
5 149. A method in accordance with claim 148 and further  
6 comprising selecting the groups using digital signals.

7  
8 150. A method of operating an integrated circuit including a  
9 receiver, a transmitter, and a frequency lock loop including a current  
10 source having a thermal voltage generator, a current controlled oscillator  
11 having a plurality of selectively engageable current mirrors multiplying  
12 up the current of the current source, the frequency of oscillation of the  
13 frequency lock loop varying in response to selection of the current  
14 mirrors, the method comprising engaging selected current mirrors and  
15 operating transistors in the current mirrors in a subthreshold mode.

16  
17 151. A method in accordance with claim 150 and further  
18 comprising arranging the current mirrors in selectable groups of varying  
19 numbers of transistors to define a binary weighting scheme.

20  
21 152. A method in accordance with claim 151 and further  
22 comprising selecting the groups using signals on digital select lines.  
23  
24

1 153. An amplifier powered by a selectively engageable voltage  
2 source, the amplifier comprising:

3 first and second electrodes for receiving an input signal to be  
4 amplified, the input electrodes being adapted to be respectively  
5 connected to coupling capacitors;

6 a differential amplifier having inputs respectively connected to the  
7 first and second electrodes, and having an output;

8 selectively engageable resistances between the voltage source and  
9 respective inputs of the differential amplifier and defining, with the  
10 coupling capacitors, the high pass characteristics of the circuit; and

11 second selectively engageable resistances between the voltage  
12 source and respective inputs of the differential amplifier, the second  
13 resistances respectively having smaller values than the first mentioned  
14 resistances, the second resistances being engaged then disengaged in  
15 response to the voltage source being engaged.

16  
17 154. An amplifier in accordance with claim 152 and further  
18 comprising coupling capacitors respectively connected to the first and  
19 second electrodes.

20  
21 155. An amplifier in accordance with claim 152 and further  
22 comprising a voltage divider, and wherein the first mentioned and  
23 second resistances are connected to the voltage source via the voltage  
24 divider.

1 156. An amplifier in accordance with claim 152 wherein the first  
2 mentioned resistances comprise respective transistors.

3  
4 157. An amplifier in accordance with claim 152 wherein the first  
5 mentioned resistances comprise respective p-type transistors.

6  
7 158. An amplifier in accordance with claim 152 wherein the  
8 second resistances comprise respective transistors.

9  
10 159. An amplifier in accordance with claim 152 wherein the  
11 second resistances comprise respective p-type transistors.  
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1 160. A radio frequency identification device comprising:  
2 an integrated circuit including a microprocessor, a receiver  
3 receiving radio frequency commands from an interrogation device, and  
4 a transmitter transmitting a signal identifying the device to the  
5 interrogator, the integrated circuit switching between a sleep mode, and  
6 a microprocessor on mode, in which more power is consumed than in  
7 the sleep mode, if the microprocessor determines that a signal received  
8 by the receiver is a radio frequency command from an interrogation  
9 device, the integrated circuit further including an amplifier powered by  
10 a selectively engageable voltage source engaged in the microprocessor  
11 on mode but not in the sleep mode, the amplifier including first and  
12 second electrodes for receiving an input signal to be amplified, the  
13 input electrodes being adapted to be respectively connected to coupling  
14 capacitors, a differential amplifier having inputs respectively connected  
15 to the first and second electrodes, and having an output, selectively  
16 engageable resistances between the voltage source and respective inputs  
17 of the differential amplifier, second selectively engageable resistances  
18 between the voltage source and respective inputs of the differential  
19 amplifier, the second resistances respectively having smaller values than  
20 the first mentioned resistances, the second resistances being engaged  
21 then disengaged in response to the integrated circuit switching from the  
22 sleep mode to the microprocessor on mode.  
23  
24

1 161. A radio frequency identification device in accordance with  
2 claim 160 and further comprising coupling capacitors respectively  
3 connected to the first and second electrodes.  
4

5 162. A radio frequency identification device in accordance with  
6 claim 160 and further comprising a voltage divider, and wherein the  
7 first mentioned and second resistances are connected to the voltage  
8 source via the voltage divider.  
9

10 163. A radio frequency identification device in accordance with  
11 claim 160 wherein the first mentioned resistances comprise respective  
12 transistors.  
13

14 164. A radio frequency identification device in accordance with  
15 claim 160 wherein the first mentioned resistances comprise respective p-  
16 type transistors.  
17

18 165. A radio frequency identification device in accordance with  
19 claim 160 wherein the second resistances comprise respective transistors.  
20

21 166. A radio frequency identification device in accordance with  
22 claim 160 wherein the second resistances comprise respective p-type  
23 transistors.  
24

1 167. A method of speeding power up of an amplifier stage  
2 powered by a voltage source and including first and second electrodes  
3 for receiving an input signal to be amplified, the input electrodes being  
4 adapted to be respectively connected to coupling capacitors; a  
5 differential amplifier having inputs respectively connected to the first and  
6 second electrodes, and having an output; and selectively engageable  
7 resistances between the voltage source and respective inputs of the  
8 differential amplifier, the method comprising:

9 shorting around the selectively engageable resistances for a  
10 predetermined amount of time in response to the voltage source being  
11 engaged.  
12

13 168. A method in accordance with claim 167 wherein the shorting  
14 step comprises engaging selectively engageable second resistances  
15 respectively connected in parallel with the first mentioned resistances  
16 and having respective resistance values lower than the first mentioned  
17 resistances.  
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1 169. A radio frequency communications system comprising:  
2 an antenna;  
3 an integrated circuit including a receiver having a Schottky diode  
4 detector including a Schottky diode having an anode coupled to the  
5 antenna and having a cathode, the Schottky diode detector further  
6 including a capacitor connected between the cathode and ground, and  
7 including a capacitor having a first contact connected to the cathode  
8 and having a second contact defining an output of the Schottky diode  
9 detector, the integrated circuit further including a clock recovery circuit  
10 recovering a clock from rising edges only of a signal at the output of  
11 the Schottky diode detector; and  
12 a current source connected to drive current through the antenna  
13 and the Schottky diode in a direction from the anode to the cathode.  
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1 170. A radio frequency communications system comprising:  
2 an antenna;  
3 an integrated circuit including a receiver having a Schottky diode  
4 detector including a Schottky diode having a cathode coupled to the  
5 antenna and having an anode, the Schottky diode detector further  
6 including a capacitor connected between the anode and ground, and  
7 including a capacitor having a first contact connected to the anode and  
8 having a second contact defining an output of the Schottky diode  
9 detector, the integrated circuit further including a clock recovery circuit  
10 recovering a clock from falling edges only of a signal at the output of  
11 the Schottky diode detector; and  
12 a current source connected to drive current through the antenna  
13 and the Schottky diode in a direction from the anode to the cathode.  
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1 171. A method of recovering a clock in a radio frequency  
2 communications system, the method comprising:

3 providing an antenna;

4 providing a receiver having a Schottky diode detector including a  
5 Schottky diode having an anode coupled to the antenna and having a  
6 cathode, the Schottky diode detector further including a capacitor  
7 connected between the cathode and ground, and including a capacitor  
8 having a first contact connected to the cathode and having a second  
9 contact defining an output of the Schottky diode detector;

10 driving current through the antenna and the Schottky diode in a  
11 direction from the anode to the cathode; and

12 recovering a clock from rising edges only of a signal at the  
13 output of the Schottky diode detector.  
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1 172. A method of recovering a clock in a radio frequency  
2 communications system, the method comprising:

3 providing an antenna;

4 providing a receiver having a Schottky diode detector including a  
5 Schottky diode having a cathode coupled to the antenna and having an  
6 anode, the Schottky diode detector further including a capacitor  
7 connected between the anode and ground, and including a capacitor  
8 having a first contact connected to the anode and having a second  
9 contact defining an output of the Schottky diode detector;

10 driving current through the antenna and the Schottky diode in a  
11 direction from the anode to the cathode; and

12 recovering a clock from falling edges only of a signal at the  
13 output of the Schottky diode detector.  
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1 173. A stage for a voltage controlled oscillator, the stage  
2 comprising:

3 a first transistor having a control electrode defining a first input,  
4 and having first and second power electrodes, the first power electrode  
5 defining a first node;

6 a second transistor having a control electrode defining a second  
7 input, and having first and second power electrodes, the first power  
8 electrode of the second transistor defining a second node;

9 a current source connected to the second power electrodes of the  
10 first and second transistors and directing current away from the second  
11 power electrodes of the first and second transistors; and

12 means defining a variable resistance connecting the first and  
13 second nodes to a supply voltage.

1 174. A stage for a voltage controlled oscillator, the stage  
2 comprising:

3 a first p-channel transistor having a gate defining a control node,  
4 having a source adapted to be connected to a supply voltage, and  
5 having a drain;

6 a second p-channel transistor having a gate connected to the  
7 control node, having a source connected to the supply voltage, and  
8 having a drain;

9 a first n-channel transistor having a gate defining a first input,  
10 having a drain connected to the drain of the first p-channel transistor  
11 and defining a first node, and having a source;

12 a second n-channel transistor having a gate defining a second  
13 input, having a drain connected to the drain of the second p-channel  
14 transistor and defining a second node, and having a source;

15 a current source connected to the sources of the first and second  
16 n-channel transistors directing current from the sources of the first and  
17 second n-channel transistors;

18 a first resistor connected between the supply voltage and the drain  
19 of the first n-type transistor;

20 a second resistor connected between the supply voltage and drain  
21 of the second n-type transistor;

22 a first source follower having an input connected to the first node  
23 and having an output defining a first output of the stage; and  
24

1 a second source follower having an input connected to the second  
2 node and having an output defining a second output of the stage.

3  
4 175. A transmitter including a ring oscillator having a chain of  
5 stages, each stage comprising:

6 a first p-channel transistor having a gate defining a control node,  
7 having a source adapted to be connected to a supply voltage, and  
8 having a drain;

9 a second p-channel transistor having a gate connected to the  
10 control node, having a source connected to the supply voltage, and  
11 having a drain;

12 a first n-channel transistor having a gate defining a first input,  
13 having a drain connected to the drain of the first p-channel transistor  
14 and defining a first node, and having a source;

15 a second n-channel transistor having a gate defining a second  
16 input, having a drain connected to the drain of the second p-channel  
17 transistor and defining a second node, and having a source;

18 a current source connected to the sources of the first and second  
19 n-channel transistors directing current from the sources of the first and  
20 second n-channel transistors;

21 a first resistor connected between the supply voltage and the drain  
22 of the first n-type transistor;

23 a second resistor connected between the supply voltage and drain  
24 of the second n-type transistor;

1 a first source follower having an input connected to the first node  
2 and having an output defining a first output of the stage; and

3 a second source follower having an input connected to the second  
4 node and having an output defining a second output of the stage.  
5

6 176. A method of varying frequency in a stage of a voltage  
7 controlled oscillator having two input transistors having gates defining  
8 input nodes and having drain to source paths adapted to be connected  
9 between a supply voltage and a current source, the method comprising  
10 providing an impedance between the input transistors and the supply  
11 voltage, and varying the impedance.  
12

13 177. A frequency doubler comprising:

14 a first Gilbert cell;

15 a second Gilbert cell coupled to the first Gilbert cell;

16 a frequency generator configured to apply a first sinusoidal wave  
17 to the first Gilbert cell; and

18 a phase shifter applying a sinusoidal wave shifted from the first  
19 sinusoidal wave to the second Gilbert cell.  
20  
21  
22  
23  
24

1 178. A frequency doubler comprising:

2 a first Gilbert cell including a first pair of transistors having  
3 sources that are connected together, a second pair of transistors having  
4 sources that are connected together, a first one of the transistors of the  
5 first pair having a gate defining a first input node and a first one of  
6 the transistors of the second pair having a gate connected to the first  
7 input node, a second one of the transistors of the first pair having a  
8 gate defining a second input node and a second one of the transistors  
9 of the second pair having a gate connected to the second input node,  
10 the first transistor of the first pair having a drain, and the second  
11 transistor of the second pair having a drain connected to the drain of  
12 the first transistor of the first pair, the second transistor of the first  
13 pair having a drain, and the first transistor of the second pair having  
14 a drain connected to the drain of the second transistor of the first  
15 pair, a third pair including first and second transistors having sources  
16 coupled together, the first transistor of the third pair having a drain  
17 connected to the source of the second transistor of the first pair, the  
18 second transistor of the third pair having a drain connected to the  
19 source of the second transistor of the second pair, and a current source  
20 connected to the sources of the third pair and forward biasing the third  
21 pair, the second transistor of the third pair having a gate defining a  
22 third input node, and the first transistor of the third pair having a gate  
23 defining a fourth input node; and  
24

1 a second Gilbert cell including a first pair of transistors having  
2 sources that are connected together, a second pair of transistors having  
3 sources that are connected together, a first one of the transistors of the  
4 first pair of the second cell having a gate defining a first input node  
5 and a first one of the transistors of the second pair of the second cell  
6 having a gate connected to the first input node of the second cell, a  
7 second one of the transistors of the first pair of the second cell having  
8 a gate defining a second input node of the second cell and a second  
9 one of the transistors of the second pair of the second cell having a  
10 gate connected to the second input node of the second cell, the first  
11 transistor of the first pair of the second cell having a drain, and the  
12 second transistor of the second pair of the second cell having a drain  
13 connected to the drain of the first transistor of the first pair of the  
14 second cell, the second transistor of the first pair of the second cell  
15 having a drain, and the first transistor of the second pair of the second  
16 cell having a drain connected to the drain of the second transistor of  
17 the first pair of the second cell, a third pair including first and second  
18 transistors having sources coupled together, the first transistor of the  
19 third pair of the second cell having a drain connected to the source of  
20 the second transistor of the first pair of the second cell, the second  
21 transistor of the third pair of the second cell having a drain connected  
22 to the source of the second transistor of the second pair of the second  
23 cell, and a current source connected to the sources of the third pair  
24 of the second cell and forward biasing the third pair of the second cell,



1 the second transistor of the third pair of the second cell having a gate  
2 defining a third input node of the second cell, and the first transistor  
3 of the third pair of the second cell having a gate defining a fourth  
4 input node of the second cell; the drain of the second transistor of the  
5 first pair of the second cell being connected to the drain of the second  
6 transistor of the first pair of the first cell, the drain of the second  
7 transistor of the second pair of the second cell being connected to the  
8 drain of the second transistor of the second pair of the second cell, the  
9 first input node of the second cell being connected to the fourth input  
10 node of the first cell, the third input node of the second cell being  
11 connected to the second input node of the first cell, and the fourth  
12 input node of the second cell being connected to the first input node  
13 of the first cell.

14  
15 179. A method of doubling frequency without using a feedback  
16 loop, the method comprising:

17 providing a first Gilbert cell;  
18 providing a second Gilbert cell coupled to the first Gilbert cell;  
19 applying a first sinusoidal wave to the first Gilbert cell; and  
20 applying a sinusoidal wave shifted from the first sinusoidal wave  
21 to the second Gilbert cell.

1 180. A pseudo random number generator comprising:  
2 a linear feedback shift register switchably operable in a first  
3 mode, and in a second mode wherein the shift register consumes more  
4 power than in the first mode.

5  
6 181. A method of generating a pseudo random number, the  
7 method comprising:

8 providing a linear feedback shift register;  
9 providing an oscillator which generates clock signals used by the  
10 linear feedback shift register for shifting; and  
11 providing a first power level to the oscillator when a pseudo  
12 random number is required, and providing a second power level, lower  
13 than the first power level, to the oscillator at other times.

14  
15 182. A method of generating a pseudo random number, the  
16 method comprising:

17 providing a linear feedback shift register;  
18 providing an oscillator which generates clock signals used by the  
19 linear feedback shift register for shifting; and operating the oscillator at  
20 a first frequency in response to a request for a pseudo random number,  
21 and operating the oscillator at a second frequency lower than the first  
22 frequency after the pseudo random number is generated.  
23  
24

1 183. A method in accordance with claim 182 and further  
2 comprising supplying power to the oscillator from a thermal voltage  
3 generator to cause the oscillator to operate at the second frequency.

4  
5 184. A system comprising:

6 a microprocessor operating at a frequency;

7 a linear feedback shift register operable in a low power mode,  
8 wherein the shift register operates at a frequency below the frequency  
9 of the microprocessor, and a high power mode wherein the shift register  
10 consumes more power than in the low power mode, operates at the  
11 frequency of the microprocessor, and shifts data into the microprocessor.

1 185. A radio frequency identification device comprising:  
2 an integrated circuit including a receiver, a transmitter, a thermal  
3 voltage generator, a microprocessor operating at a frequency, a linear  
4 feedback shift register operable in a low power mode, wherein the shift  
5 register operates at a frequency below the frequency of the  
6 microprocessor, and a high power mode wherein the shift register  
7 consumes more power than in the low power mode, operates at the  
8 frequency of the microprocessor, and shifts data into the microprocessor,  
9 an oscillator supplying clock signals to the shift register, and current  
10 mirrors supplying current to each stage of the shift register, the current  
11 mirrors being referenced to the thermal voltage generator when the shift  
12 register is in the low power mode, and, when the shift register is in  
13 the high power mode, connected to a supply voltage potential greater  
14 than the potential provided by the thermal voltage generator.  
15  
16  
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24

1 186. A method of generating a pseudo random number, the  
2 method comprising:

3 providing a thermal voltage generator, a linear feedback shift  
4 register, an oscillator supplying clock signals to the shift register, and  
5 current mirrors supplying current to each stage of the shift register;

6 referencing the current mirrors to the thermal voltage generator  
7 when no pseudo random number is required; and

8 connecting the current mirrors to a supply voltage potential  
9 greater than the potential provided by the thermal voltage generator  
10 when a pseudo random number is required.

11  
12 187. An integrated circuit comprising a receiver and a transmitter  
13 sharing a common antenna.

14  
15 188. A method of using an integrated circuit including a receiver  
16 and a transmitter, the method comprising connecting the receiver and  
17 transmitter to a common antenna.

1 189. An integrated circuit comprising:  
2 a die including a transmitter having an antenna output and a  
3 detector having an antenna input;  
4 a package housing the die;  
5 a first contact connected to the antenna output and accessible  
6 from outside the package;  
7 a second contact connected to the antenna input and accessible  
8 from outside the package; and  
9 a short electrically connecting the first contact to the second  
10 contact outside the package.  
11

12 190. A method of using an integrated circuit including a die  
13 having a transmitter including an antenna output and a detector  
14 including an antenna input, the integrated circuit further including a  
15 package housing the die, a first contact connected to the antenna  
16 output and accessible from outside the package, and a second contact  
17 connected to the antenna input and accessible from outside the package,  
18 the method comprising:

19 electrically shorting the first contact to the second contact outside  
20 the package.  
21  
22  
23  
24

1 191. A transceiver comprising:  
2 an antenna having a first end connected to a bias voltage, and  
3 having a second end;  
4 a detector including a Schottky diode having an anode connected  
5 to the second end of the antenna; and  
6 a transmitter having an output connected to the second end of  
7 the antenna.  
8

9 192. A transceiver in accordance with claim 191 wherein the  
10 Schottky diode has a cathode, and further comprising a current source  
11 directing current in the direction from the anode to the cathode.  
12

13 193. A transceiver in accordance with claim 191 wherein the  
14 receiver and transmitter do not operate simultaneously.  
15

16 194. A transceiver in accordance with claim 191 wherein the  
17 Schottky diode has a cathode, and wherein the detector and transmitter  
18 do not operate simultaneously, the transceiver further comprising a  
19 current source directing current in the direction from the anode to the  
20 cathode, and a pullup transistor connected to the cathode and  
21 configured to connect the cathode to the bias voltage when the  
22 transmitter is operating.  
23  
24

1 195. A radio frequency identification device comprising:

2 an integrated circuit including both a receiver and a transmitter;

3 a first antenna connected to the receiver; and

4 a second antenna connected to the transmitter.

5  
6 196. A radio frequency identification device in accordance with  
7 claim 195 wherein the receiver includes a Schottky diode having a  
8 cathode and an anode, and further comprising a current source directing  
9 current in the direction from the anode to the cathode.

10  
11 197. A radio frequency identification device in accordance with  
12 claim 195 wherein the receiver and transmitter do not operate  
13 simultaneously.

14  
15 198. A transceiver comprising:

16 a loop antenna having a first end connected to a bias voltage,  
17 and having a second end;

18 a second antenna;

19 a detector including a Schottky diode having an anode connected  
20 to the second end of the antenna; and

21 a transmitter having an output connected to the second antenna.  
22  
23  
24



1 199. A transceiver in accordance with claim 198 wherein the  
2 Schottky diode has a cathode, and further comprising a current source  
3 directing current in the direction from the anode to the cathode.  
4

5 200. A transceiver in accordance with claim 198 wherein the  
6 receiver and transmitter do not operate simultaneously.  
7

8 201. A transceiver comprising:

9 an antenna having a first end connected to a bias voltage, and  
10 having a second end;

11 a detector including a Schottky diode having an anode connected  
12 to the second end of the antenna; and

13 an active transmitter having an output connected to the second  
14 end of the antenna.  
15

16 202. A transceiver in accordance with claim 201 wherein the  
17 Schottky diode has a cathode, and further comprising a current source  
18 directing current in the direction from the anode to the cathode.  
19

20 203. A transceiver in accordance with claim 201 wherein the  
21 receiver and transmitter do not operate simultaneously.  
22  
23  
24

1       204. A transceiver in accordance with claim 201 wherein the  
2 Schottky diode has a cathode, and wherein the detector and transmitter  
3 do not operate simultaneously, the transceiver further comprising a  
4 current source directing current in the direction from the anode to the  
5 cathode, and a pullup transistor connected to the cathode and  
6 configured to connect the cathode to the bias voltage when the  
7 transmitter is operating.

8  
9       205. A transceiver comprising:  
10       an antenna having a first end, and having a second end;  
11       a detector including a Schottky diode having a cathode connected  
12 to the second end of the antenna and defining a potential at the  
13 second end of the antenna, the first end of the antenna being  
14 connected to a potential lower than the potential of the second end of  
15 the antenna; and

16       a backscatter transmitter including a transistor having a first power  
17 electrode connected to the first end of the antenna, a second power  
18 electrode connected to the second end of the antenna, and a control  
19 electrode adapted to have a modulation signal applied thereto.

20  
21       206. A transceiver in accordance with claim 205 and further  
22 comprising a current source directing current in the direction from the  
23 anode to the cathode.

1        207. A transceiver in accordance with claim 205 wherein the  
2 receiver and transmitter do not operate simultaneously.

3  
4        208. A transceiver in accordance with claim 205 and further  
5 comprising an integrated circuit package housing the detector and  
6 transmitter, and wherein the antenna is external of the package.

7  
8        209. A transceiver comprising:

9        a loop antenna having a first end connected to a bias voltage,  
10 and having a second end;

11       a detector including a Schottky diode having an anode connected  
12 to the second end of the antenna;

13       a backscatter transmitter having a first output and having a  
14 second output;

15       a capacitor connected between the first output and the first end  
16 of the antenna; and

17       a capacitor connected between the second output and the second  
18 end of the antenna.

19  
20       210. A transceiver in accordance with claim 209 wherein the  
21 Schottky diode has a cathode, and further comprising a current source  
22 directing current in the direction from the anode to the cathode.  
23  
24

1        211. A transceiver in accordance with claim 209 wherein the  
2 receiver and transmitter do not operate simultaneously.

3  
4        212. A transceiver in accordance with claim 209 and further  
5 comprising an integrated circuit package housing the detector and  
6 transmitter, and wherein the first and second capacitors are external of  
7 the package.

8  
9        213. A method of configuring a transceiver including a backscatter  
10 transmitter having first and second outputs, and a detector having a  
11 Schottky diode including an anode, the method comprising:

12        applying a bias voltage to a first end of an antenna;

13        connecting a second end of the antenna to the anode;

14        connecting a capacitor between the first output and the first end  
15 of the antenna; and

16        connecting a capacitor between the second output and the second  
17 end of the antenna.

18  
19        214. A method in accordance with claim 213 wherein the  
20 Schottky diode has a cathode, and further comprising directing current  
21 in the direction from the anode to the cathode.

22  
23        215. A method in accordance with claim 213 wherein the receiver  
24 and transmitter do not operate simultaneously.

1        216. A method in accordance with claim 213 and further  
2 comprising housing the detector and transmitter in an integrated circuit  
3 package, and connecting the first and second capacitors external of the  
4 package.

5  
6        217. A method of arranging a transceiver including a backscatter  
7 transmitter and a detector having a Schottky diode including a cathode,  
8 the method comprising:

9        connecting a first end of an antenna to a ground potential;  
10       connecting a second end of the antenna to the cathode; and  
11       connecting a first power electrode of a transistor to the first end  
12 of the antenna;

13       connecting a second power electrode connected to the second end  
14 of the antenna; and

15       connecting a control electrode of the transistor to a modulation  
16 signal.

17  
18       218. A method in accordance with claim 217 and further  
19 comprising a current source directing current in the direction from the  
20 anode to the cathode.

21  
22       219. A method in accordance with claim 217 wherein the receiver  
23 and transmitter do not operate simultaneously.  
24

1        220. A method in accordance with claim 217 and further  
2 comprising housing the detector and transmitter in an integrated circuit  
3 package, and locating the antenna external of the package.

4  
5        221. A method of determining when a phase lock loop achieves  
6 frequency lock relative to a desired frequency, the phase lock loop  
7 including a voltage controlled oscillator having a control node and  
8 oscillating at a frequency responsive to the voltage applied to the  
9 control node, the method comprising:

10        crossing the voltage that would result in the phase lock loop  
11 tracking the desired frequency in a first direction;

12        crossing the voltage that would result in the phase lock loop  
13 tracking the desired frequency in a second direction opposite the first  
14 direction; and

15        indicating that frequency lock has been achieved.

16  
17        222. A method in accordance with claim 221 and further  
18 comprising adjusting the voltage in the first direction after the second  
19 mentioned crossing step and before the indicating step.

20  
21        223. A method in accordance with claim 221 wherein the first  
22 mentioned crossing comprises adjusting, using steps, the voltage applied  
23 to the control node.

1        224. A method in accordance with claim 223 wherein the second  
2 mentioned crossing comprises adjusting the voltage applied to the control  
3 node using steps smaller than the steps used in the first mentioned  
4 crossing.

5  
6        225. A method in accordance with claim 221 and further  
7 comprising adjusting the voltage in the first direction after the second  
8 mentioned crossing step and before the indicating step, and wherein the  
9 adjusting comprises using a step smaller than the steps used in the first  
10 mentioned crossing.

1 226. A method of determining when frequency lock occurs  
2 relative to a desired frequency, the method comprising:

3 providing a phase lock loop including a voltage controlled  
4 oscillator that oscillates at a frequency responsive to voltage applied to  
5 the voltage controlled oscillator;

6 applying a voltage to the voltage controlled oscillator to produce  
7 a frequency of oscillation less than the desired frequency;

8 increasing the voltage applied to the voltage controlled oscillator  
9 using one or more steps of a first size;

10 increasing the voltage applied to the voltage controlled oscillator  
11 using one or more steps of a second size smaller than the first size;

12 decreasing the voltage applied to the voltage controlled oscillator  
13 using one or more steps of a third size smaller than the second size;

14 increasing the voltage applied to the voltage controlled oscillator  
15 using a step of the third size; and

16 indicating that lock has occurred in response to the increase of  
17 the step of the third size.

18  
19 227. A method in accordance with claim 226 wherein the phase  
20 lock loop tracks a timing signal.  
21  
22  
23  
24



1       228. A method in accordance with claim 226 wherein the voltage  
2 controlled oscillator has a control node, and wherein the voltage  
3 controlled oscillator oscillates at a frequency responsive to the voltage  
4 applied to the control node.

5  
6       229. A method of determining when a phase lock loop achieves  
7 frequency lock relative to a desired frequency, the phase lock loop  
8 including a voltage controlled oscillator having a control node and  
9 oscillating at a frequency responsive to the voltage applied to the  
10 control node, the method comprising:

11       increasing the voltage applied to the control node to a voltage  
12 above the voltage that would result in the phase lock loop tracking the  
13 desired frequency;

14       decreasing the voltage applied to the control node to a voltage  
15 below the voltage that would result in the phase lock loop tracking the  
16 desired frequency; and

17       increasing the voltage applied to the control node and indicating  
18 that frequency lock has been achieved.

19  
20       230. A method in accordance with claim 229 wherein the first  
21 mentioned increasing of the voltage applied to the control node  
22 comprises increasing in steps the voltage applied to the control node.

1           231. A method in accordance with claim 230 wherein the  
2 decreasing of the voltage applied to the control node comprises  
3 decreasing the voltage applied to the control node using steps smaller  
4 than the steps used in the first mentioned increasing of the voltage  
5 applied to the control node.  
6

7           232. A method in accordance with claim 230 wherein the second  
8 mentioned increasing of the voltage applied to the control node  
9 comprises increasing the voltage applied to the control node using a  
10 step smaller than the steps used in the first mentioned increasing of the  
11 voltage applied to the control node.  
12

13           233. A radio frequency identification device comprising:  
14 an integrated circuit including a microprocessor, a transmitter, and  
15 a receiver, the integrated circuit periodically switching between a sleep  
16 mode, and a receiver-on mode in which more power is consumed than  
17 in the sleep mode, and further including a selectively engageable timer  
18 preventing switching from the sleep mode to the receiver-on mode for  
19 a predetermined amount of time.  
20

21           234. A radio frequency identification device in accordance with  
22 claim 233 wherein the timer is a countdown timer.  
23  
24

1        235. A radio frequency identification device in accordance with  
2 claim 233 wherein the timer comprises a counter.

3  
4        236. A radio frequency identification device in accordance with  
5 claim 233 wherein the timer is set by a radio frequency signal received  
6 by the receiver.

7  
8        237. A radio frequency identification device comprising:  
9 an integrated circuit including a microprocessor, a transmitter, and  
10 a receiver, the integrated circuit periodically switching between a sleep  
11 mode, and a receiver-on mode in which more power is consumed than  
12 in the sleep mode, and further including means for selectively preventing  
13 switching from the sleep mode to the receiver-on mode for a  
14 predetermined amount of time.

15  
16        238. A radio frequency identification device in accordance with  
17 claim 237 wherein the means comprises a countdown timer.

18  
19        239. A radio frequency identification device in accordance with  
20 claim 237 wherein the means comprises a counter.

21  
22        240. A radio frequency identification device in accordance with  
23 claim 237 wherein the means prevents switching from the sleep mode  
24 in response to a radio frequency signal received by the receiver.

1           241. A radio frequency identification device comprising:  
2           an integrated circuit including a microprocessor, a transmitter, and  
3           a receiver, the integrated circuit being switchable between a sleep mode,  
4           and a mode in which more power is consumed than in the sleep mode,  
5           the integrated circuit being switched from the sleep mode to the mode  
6           in which more power is consumed in response to a direct sequence  
7           spread spectrum modulated radio frequency signal being received by the  
8           receiver which has a predetermined number of transitions within a  
9           certain period of time, the integrated circuit further including a  
10          selectively engageable timer which prevents switching from the sleep  
11          mode for a period of time regardless of whether a signal is  
12          subsequently received by the receiver which has the predetermined  
13          number of transitions within a certain period of time.

14  
15          242. A radio frequency identification device in accordance with  
16          claim 241 wherein the timer is a countdown timer.

17  
18          243. A radio frequency identification device in accordance with  
19          claim 241 wherein the timer comprises a counter.

20  
21          244. A radio frequency identification device in accordance with  
22          claim 241 wherein the timer is set by a radio frequency signal received  
23          by the receiver.  
24

1           245. A method for conserving power in a radio frequency  
2 identification device, the method comprising:

3           periodically switching from a sleep mode to a receiver on mode  
4 and performing tests to determine whether to further switch to a  
5 microprocessor on mode because a valid radio frequency signal is  
6 present; and

7           selectively disabling the periodic switching from the sleep mode for  
8 a predetermined amount of time.

9  
10          246. A method for conserving power in accordance with  
11 claim 245 wherein the selective disabling is performed in response to  
12 a radio frequency command.

13  
14          247. A method for conserving power in accordance with claim  
15 245 wherein the selective disabling is performed in response to a radio  
16 frequency command, and wherein the selective disabling cannot be  
17 cancelled by a subsequent radio frequency command.

18  
19          248. A method in accordance with claim 245 wherein the step  
20 of selectively disabling comprises setting a timer.

21  
22          249. A method in accordance with claim 245 wherein the step  
23 of selectively disabling comprises setting a countdown timer.  
24

1 250. A method in accordance with claim 245 wherein the  
2 predetermined amount of time is selected via a radio frequency  
3 command.

4  
5 251. A method in accordance with claim 245 wherein the  
6 predetermined amount of time is variable.

7  
8 252. A method in accordance with claim 245 wherein the  
9 predetermined amount of time is selectable from a number of available  
10 amounts of time.